

Dinesh Ramcharan Bhukya

Email: dineshramcharanbhukya@gmail.com
LinkedIn: linkedin.com/in/dinesh-ramcharan-bhukya
Phone: (+91) 9505276576

IIT Bhubaneswar

M.Tech – Semiconductor Technology and Chip Design
Final Year Postgraduate

Education

Year	Degree	Institute	Score
2027*	M.Tech – Semiconductor Technology and Chip Design	Indian Institute of Technology Bhubaneswar	7.14 / 10
2025	B.Tech – Electronics and Communication Engineering	JNTUH UCES, Sultanpur, Telangana	6.72 / 10
2021	Intermediate (PCM)	TTWREIS SOE Khammam	76.4%
2019	Secondary School Certificate (10 th)	Telangana Model School karepally	8.8 / 10

Internship Experience

Rudhaa Skillforge Technologies

Sep 2024 – Nov 2024

VLSI Design Engineer Intern

- Designed and verified RTL modules using Verilog and SystemVerilog, ensuring functional correctness through extensive simulation.
- Performed synthesis and post-synthesis analysis using Cadence and Xilinx Vivado to meet timing and area constraints.
- Conducted static timing analysis (STA) to identify critical paths and optimize logic performance.
- Gained hands-on exposure to industry-standard digital design and verification workflows.

Academic Projects

Optimized BCD–Binary and Binary–BCD Serial Converter

- Designed a full-custom 12-bit serial converter supporting both BCD-to-binary and binary-to-BCD conversion.
- Implemented Hamming-standard architecture using registers, memory blocks, and combinational logic.
- Verified functionality and timing using Xilinx Vivado simulations.

NMOS Input Folded Cascode Operational Amplifier Design

- Designed a folded cascode op-amp in 180 nm CMOS technology achieving 52 dB DC gain and 1 MHz UGB.
- Performed AC, DC, transient, noise, CMRR, PSRR, slew-rate, and pole-zero analyses in Cadence Virtuoso.

32-bit Leading Zero Counter Using LUTs

- Designed a 32-bit leading zero counter to detect consecutive zeros from MSB to first non-zero bit.
- Extended architecture scalability to 48-bit and 64-bit using primitive instantiation techniques.

16-bit Carry Select Adder–Subtractor

- Designed a control-signal-based adder–subtractor supporting both addition and subtraction operations. A 1-bit control signal M will decide whether to add or subtract.
- Implemented optimized 2–2–3–4–5 block configuration for reduced propagation delay.

Fabrication of N-RGO Junction Photodetector

- Fabricated a photosensitive device from material synthesis to electrical characterization.
- Demonstrated red laser light detection and evaluated device response.
- Characterized I–V behavior using Origin software.

Crypto Coprocessor Using AES and LFSR (B.Tech Project)

- Designed and implemented a crypto coprocessor for secure data encryption.
- Integrated AES algorithm with LFSR-based key generation.
- Simulated and synthesized the design using Cadence and Vivado tools.

Efficient Round Robin Arbiter (B.Tech Project)

- Developed an optimized round-robin arbiter for fair and efficient resource allocation.
- Implemented the design in Verilog and validated through simulation.

Technical Skills

HDL & Digital Design: Verilog, RTL Design

EDA Tools: Cadence Virtuoso, Cadence Innovus, Xilinx Vivado, Sentaurus, LTspice

Programming: C, Scripting Languages

Analysis: Static Timing Analysis, Logic Optimization

Fabrication Knowledge: Semiconductor Fabrication, Packaging, Testing

Other Tools: MATLAB, Image Processing, MS Office

Certifications

- VLSI Physical Design with Timing Analysis – NPTEL
- VLSI Design: RTL to GDS – NPTEL
- VLSI Digital Design and Verilog Programming – Infosys Springboard
- Design and Analysis of Digital Circuits – Alison
- Digital Communication Using GNU Radio – NPTEL
- Digital Image Processing – NPTEL
- VLSI for Beginners – NIELIT
- VLSI System-on-Chip Design Overview – Maven Silicon

Positions of Responsibility

Teaching Assistant

Aug 2025 – Present

- Conducted laboratory and tutorial sessions and assisted in evaluation of assignments and examinations.
- Supported students through academic mentoring and doubt resolution.

Team Lead – College Events

- Led organizing teams for technical and cultural events, ensuring smooth execution and coordination.

Coordinator – Photography Club (JNTUH UCES)

- Coordinated media coverage and documentation for college fests and cultural events.

Declaration

I hereby declare that the information provided above is true to the best of my knowledge.