Dinesh Ramcharan Bhukya

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Education

Indian Institute of Technology Bhubaneswar CGPA: 7.14/10
M.Tech in Semiconductor Technology and Chip Design *2025 – 2027*

JNTUH UCES, Sultanpur, Telangana CGPA: 6.72/10
B.Tech in Electronics and Communication Engineering *2021 – 2025*

TTWREIS SOE, Khammam Score: 76.4%
Intermediate (PCM) *2019 – 2021*

Technical Skills

Physical Design: RTL-to-GDSII, Floorplanning, Placement, CTS, Routing, Timing Closure, Static Timing Analysis, IR Drop Analysis, Physical Verification
EDA Tools: Cadence Innovus, Cadence Genus, Cadence Tempus, Synopsys ICC2, Synopsys Fusion Compiler, Synopsys PrimeTime
HDL & Scripting: Verilog, SystemVerilog, TCL, SDC, LEF/DEF
Simulation & Analysis: Cadence Virtuoso, Xilinx Vivado, COMSOL, MATLAB, LTspice, Origin
Technology Exposure: ASAP7nm, 5nm, 7nm, 10nm, 16nm, 20nm, 45nm, 90nm, 180nm, 3D PDK, CMOS, Semiconductor Fabrication, Advanced Packaging
Core Concepts: STA, Timing Constraints, Setup/Hold Analysis, Clock Tree Synthesis, Congestion Analysis, RC Extraction, Power Integrity, PPA Optimization, DRC

Internship Experience

VLSI Design Engineer Intern – Rudhaa Skillforge Technologies Sep 2024 – Nov 2024
VLSI Design and Verification

- Designed and verified RTL modules using **Verilog/SystemVerilog**, ensuring functional correctness through simulation and verification.
- Performed **logic synthesis and post-synthesis analysis** using Cadence and Xilinx Vivado while evaluating timing and area constraints.
- Performed **Static Timing Analysis (STA)** to identify critical paths and analyze timing performance.
- Gained hands-on exposure to **RTL-to-GDSII design flow**, digital implementation, synthesis, timing analysis, and industry-standard EDA workflows.

Projects

SHA256 Physical Design Implementation | *Cadence Innovus, ASAP7nm, TCL* 2026

- Implemented **SHA256** digital design through the complete **RTL-to-GDSII physical design flow** using **Cadence Innovus** with the **ASAP7nm** technology.
- Performed **floorplanning, tap-cell insertion, I/O pin placement, power-ring/stripe/rail generation, standard-cell placement, CTS, and signal routing** using TCL-based Innovus scripts.
- Optimized placement using **place_opt_design** and analyzed **area, power, timing, placement density, and routing quality** using Innovus PPA reporting commands.
- Executed **clock tree synthesis and detailed routing**, identified routing and DRC violations, and investigated **metal-spacing, shorts, and congestion-related issues** during post-route analysis.
- Performed post-route **timing, power, and area analysis** and design optimization using **report_timing**, **report_power**, **report_area**, and **optDesign**.

Automated 3D IC Compiler Flow for Simultaneous Timing Closure | *Innovus, Tempus, TCL, SDC* 2026

- Developing an automated **pseudo-3D physical design flow** that enables existing 2D EDA engines to perform timing-aware implementation of multi-tier 3D IC designs.
- Exploring **timing-aware tier partitioning, pseudo-3D floorplanning, placement, CTS, routing, and timing closure** using Cadence Innovus and Tempus.
- Developing TCL automation scripts and modified **SDC constraints** to represent 3D inter-tier connections using anchor-cell abstractions.
- Evaluating **Compact-2D and Cascade-2D** implementation strategies for concurrent placement, CTS, routing, and timing optimization.

RTL-to-GDSII Physical Design Flow Analysis | *Genus, Innovus, PrimeTime, TCL* 2026

- Explored the complete **RTL-to-GDSII implementation flow** including synthesis, floorplanning, placement, CTS, routing, and timing analysis.
- Worked with multiple technology environments including **ASAP7, 5nm, 7nm, 10nm, 16nm, 20nm, 45nm, 90nm, 180nm, and 3D PDK** designs for physical implementation and analysis.
- Analyzed post-implementation timing using **PrimeTime** and investigated critical paths, setup/hold violations, and timing optimization techniques.

Power Grid Optimization and IR Drop Analysis | *Cadence Innovus, TCL* 2026

- Analyzed power distribution networks and explored **IR drop optimization** through power-grid planning and power-pad/bump placement.
- Targeted a maximum IR drop of $\leq 5\%$ **of the 1.2 V VDD supply**, corresponding to a maximum allowable drop of ≤ 60 **mV**, under the specified design constraints.
- Evaluated power-grid topology, metal-layer utilization, and power-pad distribution to improve **power integrity** and minimize supply voltage degradation.

NMOS Input Folded-Cascode Operational Amplifier | *Cadence Virtuoso, 180 nm CMOS* 2025

- Designed a folded-cascode operational amplifier in **180 nm CMOS**, achieving approximately **52 dB DC gain** and **1 MHz unity-gain bandwidth**.
- Performed AC, DC, transient, noise, CMRR, PSRR, slew-rate, and pole-zero analyses using **Cadence Virtuoso**.

Optimized BCD–Binary and Binary–BCD Serial Converter | *Verilog, Xilinx Vivado* 2025

- Designed a **12-bit serial converter** supporting both BCD-to-binary and binary-to-BCD conversion using registers, memory, and combinational logic.
- Verified functional behavior and timing through **Xilinx Vivado simulation**.

Fabrication of N-RGO Junction Photodetector | *Material Synthesis, Device Fabrication, Origin* 2025

- Fabricated a photosensitive **N-RGO junction photodetector** involving material synthesis, device fabrication, and electrical characterization.
- Demonstrated **red laser light detection** and evaluated the photodetector response under optical excitation.
- Characterized the device **I–V behavior** and analyzed electrical response using **Origin software**.

Crypto Coprocessor Using AES and LFSR | *Verilog, Cadence, Vivado* 2025

- Designed and implemented a hardware **crypto coprocessor** for secure data encryption using the **AES algorithm**.
- Integrated **LFSR-based key generation** with the AES encryption architecture for hardware-oriented cryptographic processing.
- Simulated and synthesized the design using **Cadence and Xilinx Vivado** tools.

Efficient Round Robin Arbiter | *Verilog, RTL Design, Simulation* 2024

- Developed an optimized **round-robin arbiter** for fair and efficient resource allocation among multiple requesters.
- Implemented the arbitration logic in **Verilog** and validated functional behavior through simulation.

Certifications & Training

VLSI Physical Design with Timing Analysis – NPTEL
VLSI Design: RTL to GDS – NPTEL
VLSI Digital Design and Verilog Programming – Infosys Springboard
VLSI for Beginners – NIELIT
VLSI System-on-Chip Design Overview – Maven Silicon
MoTA Foundational Training in Semiconductor Technology – CeNSE, IISc

Positions of Responsibility

Teaching Assistant, IIT Bhubaneswar Aug 2025 – Present
Team Lead – College Events – Led organizing teams for technical and cultural events, coordinating planning and execution.
Coordinator – Photography Club, JNTUH UCES – Coordinated media coverage and documentation for college events.